ELECTRONIC APPARATUS

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2014-259506, filed December 22, 2014; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to an electronic apparatus.

BACKGROUND

An electronic apparatus into which a semiconductor device having a controller and a semiconductor memory is embedded is being provided.

An example of related art includes JP-A-2011-54142.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagram illustrating a system configuration of a semiconductor device according to a first embodiment.

FIG. 2 is a perspective view illustrating a case in which a semiconductor device is mounted in a host device.

FIG. 3 is a partially sectioned side view illustrating a tablet type portable computer.

FIG. 4 is a view illustrating the semiconductor device according to the first embodiment.

FIG. 5 is a sectional view illustrating a NAND memory and a controller.

FIG. 6 is a block diagram illustrating a system configuration of the controller.

FIG. 7 is a perspective view illustrating a connector unit.

FIG. 8 is a perspective view illustrating a connector unit.

FIG. 9 is a top sectional view illustrating a connector unit.

FIG. 10 is a view illustrating a main board.

FIG. 11 is a perspective view illustrating a connector unit.

FIG. 12 is a view illustrating a semiconductor device according to a second embodiment.

FIG. 13 is a sectional side view of the semiconductor device and a main board according to the second embodiment.

FIG. 14 is a sectional side view of a semiconductor device and a main board according to a third embodiment.

FIG. 15 is a sectional view illustrating an example of a connector unit, an interface unit, and a cover, according to the third embodiment.

FIG. 16 is a sectional view illustrating another example of the connector unit, the interface unit, and the cover, according to the third embodiment.

FIG. 17 is a perspective view illustrating an example of a connector unit, an interface unit according to a fourth embodiment.

FIG. 18 is a partially sectioned side view illustrating a tablet type portable computer according to a fifth embodiment.

FIG. 19 is a view illustrating a main board according to a sixth embodiment.

FIG. 20 is a view illustrating a semiconductor device and the main board according to the sixth embodiment.

DETAILED DESCRIPTION

[0004]

Exemplary embodiments realize a thin electronic apparatus.

[0007]

Hereinafter, embodiments will be described with reference to the drawings.

[0008]

In the specification, examples of a plurality of expressions are used for some elements. The examples of the expressions are merely examples, and do not deny that the elements are expressed differently from each other. In addition, elements for which a plurality of expressions is not used may also be expressed differently from each other.

[0009]

In addition, the drawings are schematic, and a relationship between a thickness and a planar dimension, a ratio of the thicknesses of each layer, or the like can be different from actual one. In addition, a section in which a relationship or a ratio between dimensions is different from each other in the drawings can be included.

First Embodiment

[0010]

FIG. 1 illustrates a system configuration of a semiconductor device 1 according to a first embodiment. The semiconductor device 1 is an example of each of a “semiconductor module” and a “semiconductor memory device”. The semiconductor device 1 according to the present embodiment is, for example, a solid state drive (SSD), but is not limited to this.

[0011]

As illustrated in FIG. 1, the semiconductor device 1 according to the present embodiment is connected to a portable computer that is an example of an electronic apparatus, or to a host device 201 (hereinafter, referred to as a host) such as a CPU core, via a memory connection interface such as an interface according to the standard, such as serial advanced technology attachment (SATA) or peripheral component interconnect express (PCIe), and functions as an external memory of the host device 201. In addition, an interface 2 may be one according to another standard.

[0012]

The semiconductor device 1 receives an electric power from the host device 201 via an interface. A CPU of a personal computer, a CPU of an imaging device, such as a still camera or a video camera, or the like can be used as the host device 201. In addition, the semiconductor device 1 can perform data communication with a debug device via a communication interface such as an RS232C interface (RS232C I/F). In addition, the semiconductor device 1 may be used as a storage device of an electronic apparatus, such as a notebook type portable computer, a tablet terminal, or a detachable notebook personal computer (PC).

[0013]

FIG. 2 is a view in a case in which the semiconductor device 1 is embedded in a detachable notebook PC. In addition, FIG. 3 is a sectional view of a display device side of the detachable notebook PC illustrated in FIG. 2, that is, a tablet type portable computer 201. In addition, the detachable notebook PC has a configuration in which the tablet type portable computer 201 and an input device 218 are connected to each other by a connection unit 219. As illustrated in FIG. 2, the semiconductor device 1 is embedded in the tablet type portable computer 201 of the detachable notebook PC. For this reason, even if the input device 218 and the display device side in the detachable notebook PC are separated from each other, only the display device side can function as the tablet type portable computer 201. In addition, the tablet type portable computer 201 is an example of an electronic apparatus, and, for example, has a size that a user can use the tablet type portable computer 201 by holding it in his hand. In this case, the tablet type portable computer 201 functions as a host device of the semiconductor device 1.

[0014]

The tablet type portable computer 201 includes a housing 202, a display module 203, the semiconductor device 1, and a main board 205. The housing 202 includes a protection plate 206, a base 207, and a frame 208. The protection plate 206 is a square plate made of glass or plastic, and configures a surface of the housing 202. The base 207 is made of a metal, such as an aluminum alloy or a magnesium alloy, and configures the bottom of the housing 202.

[0015]

The frame 208 is provided between the protection plate 206 and the base 207. The frame 208 is made of a metal, such as an aluminum alloy or a magnesium alloy, and has an embedding section 210 and a bumper section 211 which are configured as one piece. The embedding section 210 is interposed between the protection plate 206 and the base 207. According to the present embodiment, the embedding section 210 defines a first embedding space 212 between the embedding section 210 and the protection plate 206, and defines a second embedding space 213 between the embedding section 210 and the base 207.

[0016]

The bumper section 211 is formed in an outer circumference portion of the embedding section 210 as one piece with the embedding section 210, and continuously surrounds the first embedding space 212 and the second embedding space 213 in a circumferential direction. Furthermore, the bumper section 211 extends in a thickness of the housing 202 so as to be spanned between the outer circumference portion of the protection plate 206 and the outer circumference portion of the base 207, and configures the outer circumference surface of the housing 202.

[0017]

The display module 203 is contained in the first embedding space 212 of the housing 202. The display module 203 is covered by the protection plate 206, and a touch panel 214 with a handwriting input function is interposed between the protection plate 206 and the display module 203. The touch panel 214 adheres to the rear surface of the protection plate 206.

[0018]

In addition, as illustrated in FIG. 3, a plurality of first fixing sections 230 and a plurality of second fixing sections 231 are provided in the second embedding space in the housing 202. The first fixing sections 230 and the second fixing sections 231 are, for example, protrusion sections having screw holes, the main board 205 is fixed to the plurality of first fixing sections 230 by screws, and the semiconductor device 1 is fixed to the plurality of second fixing sections 231 by screws.

[0019]

In addition, by aligning the heights of the protrusion sections of the first fixing sections 230 and the second fixing sections 231, a substrate 11 of the semiconductor device 1 and a substrate 215 of the main board 205 are positioned on the substantially same plane.

[0020]

The semiconductor device 1 is contained in the second embedding space 213 of the housing 202 together with the main board 205. The semiconductor device 1 includes the substrate 11, a NAND memory 12, a controller 13, and an electronic component such as a DRAM 14.

[0021]

The substrate 11 is, for example, a printed wiring plate, and includes a first surface 11a (embedding surface) on which patterned conductors (not illustrated) are formed. Circuit components are embedded on the embedding surface 11a of the substrate 11, and are soldered to the conductor patterns.

[0022]

The main board 205 includes the substrate 215 and a plurality of circuit components 216 such as semiconductor packages, and is fixed to the first fixing section 230 of the housing 202 by screws that pass through the screw holes 217.

[0023]

The substrate 215 includes a first surface 215a (embedding surface) on which a plurality of patterned conductors (not illustrated) are formed. The circuit components 216 are embedded on the embedding surface 215a of the substrate 215, and are soldered to conductor patterns.

[0024]

The semiconductor device 1 according to the present embodiment is a single side embedding device in which circuit components such as the NAND memory 12 are embedded on only the embedding surface 11a. Thus, circuit components that protrude from an external surface are not embedded on a second surface 11b that is positioned on a side opposite to the first surface 11a. For this reason, as illustrated in FIG. 3, the semiconductor device 1 can be embedded in the tablet type portable computer 201 that requires thinning.

[0025]

FIG. 4 is a specific example of the semiconductor device 1. In FIG. 4, (a) is a plan view, (b) is a bottom surface view, and (c) is a side surface view. The semiconductor device 1 includes the substrate 11, the NAND type flash memory (hereinafter, referred to as a NAND memory) 12 that is used as a nonvolatile semiconductor memory element, the controller 13, the dynamic random access memory (DRAM) 14 that is a volatile semiconductor memory element which can perform a faster storing operation than the NAND memory 12, an oscillator 15 (OSC), an electrically erasable and programmable ROM (EEPROM) 16, a power supply circuit 17, a temperature sensor 18, and electronic components 19, such as a resistor and a capacitor.

[0026]

In addition, the NAND memory 12 and the controller 13 according to the present embodiment are embedded as a semiconductor package that is an electronic component. For example, a semiconductor package of the NAND memory 12 is a module of a system in package (SiP) type, and a plurality of semiconductor chips is sealed in one package. The controller 13 controls an operation of the NAND memory 12.

[0027]

The substrate 11 is a circuit substrate of a substantially rectangular shape that is configured by a material such as glass epoxy resin, and defines the outer dimension of the semiconductor device 1. The substrate 11 includes a first surface 11a, and a second surface 11b that is positioned on a side opposite to the first surface 11a. In the present specification, a surface other than the first surface 11a and the second surface 11b among the surfaces that configure the substrate 11 is defined as a “side surface”. The first surface 11a is a component embedding surface on which the NAND memory 12, the controller 13, the DRAM 14, the oscillator 15, the EEPROM 16, the power supply component 17, the temperature sensor 18, another electronic components 19, such as a resistor and a capacitor, and the like are embedded.

[0028]

The substrate 11 according to the present embodiment is, for example, a single surface embedding substrate, and all the components that configure the semiconductor device 1 are embedded on the first surface 11a. Meanwhile, the second surface 11b is a non-component embedding surface on which components are not embedded. By doing this, as described above, the semiconductor device 1 according to the present embodiment can be thinned, compared to a case in which substrate-mounted components that protrude from the surface are embedded on both surfaces of the substrate 11.

[0029]

In addition, here illustrates an example in which a single-surface embedding is made, but another components or functions may be added to the second surface 11b of the substrate 11 according to the present embodiment. For example, in order to easily perform performance verification of a product, a pad for test can be provided on the second surface. In this case, restriction for a high density design for providing a pad in a narrow region of the first surface 11a, adjustment of an embedded position of other components embedded on the first surface 11a, or the like is not required, and thus the degree of design freedom of pad embedding is improved. Then, a pad electrode for test can be provided on the second surface 11b that is positioned in the rear of each component which is embedded on the first surface 11a, and thereby, it is possible to shorten a wiring length for routing, and to avoid electrical loss.

[0030]

The substrate 11 is formed in a substantially rectangular shape as described above, and includes a first edge section 11c that is positioned along a lateral direction, and a second edge section 11d that is positioned on a side opposite to the first edge section 11c. The first edge section 11c includes a connector section 21 (substrate interface section, terminal section, connection section). The connector section 21 includes a plurality of concave sections 21a (metal terminals) that is used as, for example, connection terminals. The connector section 21 is electrically connected to the host device 201. The connector section 21 transmits and receives signals (control signal and data signal) to and from the host device 201.

[0031]

The connector section 21 according to the present embodiment is an interface according to the standard of, for example, PCI Express (hereinafter, referred to as PCIe). That is, a high speed signal (high speed differential signal) according to the standard of the PCIe is transferred between the connector section 21 and the host device 201. The connector section 21 may be one according to, for example, other standards. The semiconductor device 1 receives an electric power from the host device 201 via the connection section 21.

[0032]

The power supply circuit 17 is, for example, a DC-DC converter, and generates a predetermined voltage necessary for the semiconductor package 12 or the like from an electric power that is received from the host device 201. In addition, it is preferable that the power supply circuit 17 is provided in the vicinity of the connector section 21, in order to reduce loss of the electric power that is supplied from the host device 201.

[0033]

The controller 13 controls an operation of the NAND memory 12. That is, the controller 13 controls writing, reading, and erasing of data on the NAND memory 12.

[0034]

The DRAM 14 is an example of a volatile memory, and is used for storage of management information of the semiconductor memory 32, cache of data, or the like.

[0035]

The oscillator 15 supplies the controller 13 with an operation signal with a predetermined frequency. The EEPROM 16 stores a control program or the like as fixed information. The temperature sensor 18 detects temperature of the semiconductor device 1, and notifies the controller 13 of the detected temperature.

[0036]

FIG. 5 illustrates a cross section that discloses a semiconductor package which is used as the NAND memory 12, and a semiconductor package which is used as the controller 13, according to the present embodiment. The controller 13 includes a package substrate 41, a controller chip 42, a bonding wire 43, a sealing section (mold material) 44, and a plurality of solder balls 45. The NAND memory 12 includes a package substrate 31, a plurality of semiconductor memories 32, a bonding wire 33, a sealing section (mold material) 34, and a plurality of solder balls 35.

[0037]

The substrate 11 is, for example, a wiring substrate with multiple layers as described above, includes a power supply layer that is not illustrated, a ground layer, and internal wires, and electrically connects the controller chip 42 to the plurality of semiconductor memories 32 via the bonding wires 33 and 43, the plurality of solder balls 35 and 45, and the like.

[0038]

As illustrated in FIG. 5, the plurality of solder balls 35 and 45 are provided on the package substrates 31 and 41. For example, the plurality of solder balls 35 and 45 are disposed in a lattice pattern on a second surface 31b of the package substrate 31. It is not necessary for the plurality of solder balls 35 to be fully disposed on the whole of the second surface 31b of the package substrate 31, and the plurality of solder balls 35 may be partially disposed.

[0039]

In addition, fixing of the controller chip 32 to the package substrate 31, fixing of the semiconductor memory 42 to the package substrate 41, and fixing between the plurality of the semiconductor memories 42 are performed by mount films 38 and 48.

[0040]

In addition, as illustrated in FIG. 4, the controller 13 according to the present embodiment has a substantially rectangular shape, and includes a first edge section 13a in a lateral direction, a second edge section 13b that is positioned on a side opposite to the first edge section 13a, a third edge section 13c in a longitudinal direction, and a fourth edge section 13d that is positioned on a side opposite to the third edge section 13c. The second edge section 13b is positioned on the NAND memory 12 side that is mounted on the substrate 11 and is adjacent to the controller 13, and the first edge section 13a is positioned on the connector section 21 side that is included in the substrate 11.

[0041]

In addition, the solder balls 45 described above include a solder ball 45a that exists on the first edge section 13a side of the controller 13, and a solder ball 45b that exists on the second edge section 13b side. In addition, the solder balls 35 includes a solder ball 35a that is positioned on the controller 13 side, and a solder ball 35b that is positioned on a side opposite to the solder ball 35a.

[0042]

FIG. 6 illustrates an example of a system configuration of the controller 13. As illustrated in FIG. 6, the controller 13 includes a buffer 131, a central processing unit (CPU) 132, a host interface section 133, and a memory interface section 134.

[0043]

The buffer 131 temporarily stores a certain amount of data, when data that is transferred from the host device 201 is written to the NAND memory 12, or temporarily stores a certain amount of data, when data that is read from the NAND memory 12 is transferred to the host device 201.

[0044]

The CPU 132 controls the whole of the semiconductor device 1. For example, the CPU 132 receives a write command, a read command, and an erasure command from the host device 201 and access a corresponding area of the NAND memory 12, or controls data transfer processing via the buffer 131.

[0045]

The host interface section 133 is positioned between the connector section 21 of the substrate 11, and the CPU 132 and the buffer 131. The host interface section 133 performs interface processing between the controller 13 and the host device 201. For example, a PCIe high-speed signal is transferred between the host interface section 133 and the host device 201.

[0046]

In addition, the host interface section 133 is disposed in a direction of the connector section 21 of the substrate 11, that is, disposed so as to be biased to the first edge section 13a, in the controller 13. In this case, it is possible to shorten the wires between host interface section 133 and the connector section 21 of the substrate 11.

[0047]

For example, if the host interface section 133 is disposed in a direction opposite to the connector section 21, that is, disposed so as to be biased to the second edge section 13b, in the controller 13, a wiring distance is also extended by a length in a longitudinal direction of a controller chip, as can also be seen from FIG. 4. Since the wires are lengthened, a parasitic capacitance, a parasitic resistance, and a parasitic inductance increase, and it is difficult to maintain a characteristic impedance of signal wires. In addition, it can become a cause of signal delay.

[0048]

From the above viewpoint in the present embodiment, it is preferable that the host interface section 133 is disposed so as to be biased to a first edge section 13a in the controller 13, and for example, if a command is transferred from a host device, the connector section 21 receives a signal from the host device 201, and performs signal communication with the host interface section 133 via the solder ball 45a from patterned wires of the substrate 11. According to this, operational stability of the semiconductor device 1 is increased.

[0049]

In addition, it is preferable that an electronic component is not embedded between the host interface section 133 and the connector section 21 of the substrate 11.

[0050]

As described above, if a wiring distance between the host interface section 133 and the connector section 21 is long, there occurs a problem that it is difficult to maintain an impedance of a signal wire, and in addition, a signal is delayed, or the like. Thus, it is not preferable that an electronic component is embedded between the host interface section 133 and the connector section 21, in order to form a wire that connects the host interface section 133 to the connector section 21 in a shortest distance, that is, to form in a straight line.

[0051]

In addition, there is a possibility that an electronic component, such as the power supply circuit 17 or the DRAM 14 is accompanied by noise at the time of operation. As the electronic component is not embedded between the host interface section 133 and the connector section 21, there is a low possibility that signals which are transferred between the host interface section 133 and the connector section 21 is accompanied by noise, and thus, the operational stability of the semiconductor device 1 can be increased.

[0052]

The memory interface section 134 is positioned between the NAND memory 12, and the CPU 132 and the buffer 131. The memory interface section 134 performs interface processing between the controller 13 and the NAND memory 12.

[0053]

In the present embodiment, the memory interface section 134 is disposed in a side opposite to the connector section 21 of the substrate 11, that is, disposed so as to be biased to the second edge section 13b side, in the controller 13. In this case, it is possible to shorten a wiring distance between the memory interface section 134 and the NAND memory 12.

[0054]

A signal that is transferred from the controller 13 is transferred to the patterned wires of the substrate 11 via the solder ball 45b, and is transferred to the semiconductor memory 32 from the solder ball 35a. According to this, a wiring distance is shortened, and operational stability of the semiconductor device 1 is increased.

[0055]

In addition, it is preferable that the power supply circuit 17, the DRAM 14, or the like is not embedded also between the memory interface section 134 of the controller 13 and the NAND memory 12 on the substrate 11. This is for reducing the possibility that signals which are transferred between the memory interface section 134 and the connector section 21 are accompanied by noise, and for increasing operational stability of the semiconductor device 1.

[0056]

FIG. 7 and FIG. 8 are perspective views of the connector sections 21 in the semiconductor device 1 according to the present embodiment. As illustrated in FIG. 7, the connector section 21 in the present embodiment includes, for example, a plurality of first concave sections 21a. In addition, the connector section 21 has a structure in which a surface of a conductive layer 20 of the substrate 11 is partially exposed, and a plurality of first plating sections 21b are provided on the surface of the exposed conductive layers 20 in side surfaces of the first concave sections 21a, as illustrate in FIG. 8. The first plating sections 21b are plated with, for example, gold, but are not limited to this. In addition, the gold plating is not necessarily required, and the conductive layer 20 may be in an exposed state. Furthermore, the conductive layer 20 that is exposed on the side surface of the first concave section 21a may not necessarily be a layer shape, and a portion that is electrically connected to the conductive layer 20 may be exposed from the side surface, in a state like a signal line, for example.

[0057]

In addition, the connector section 21 may have a structure in which an elastic material 310 is included, between the first plating section (first metal section) 21b and the side surface of the substrate 11, in a state of being electrically connected to the conductive layer 20. In addition, for example, rubber, urethane, silicon elastomer, or the like is used for the elastic material 310.

[0058]

FIG. 9 illustrates a top sectional view of the connector section 21, when an elastic material is interposed between the first metal section 21b and the substrate 11. In addition, in FIG. 9, the first metal section 21b is provided at a position only in a lateral direction of the substrate 11, in the first concave section 21a, but is not limited to this.

[0059]

In addition, as described above, the first metal section 21b is required to be electrically connected to the conductive layer 20, but, for example, a signal line may be electrically connected via the center of the elastic material 310, and the exposed conductive layer 20 and the first metal section 21b may be in contact with each other, in a portion which is not covered with the elastic material 310.

[0060]

In this case, the interface section 221 is pressed by the connector section 21 according to the elastic force of the elastic material 310, and thereby stability of electric connection is increased.

[0061]

FIG. 10 is a view illustrating the main board 205 that is mounted in the host device 201 to which the semiconductor device 1 is connected. The main board 205 includes a substrate 215, and the substrate 215 includes a first surface 215a, and a second surface 215b that is positioned on a side opposite to the first surface 215a. In addition, the substrate 215 is a multi-layer wiring plate, and includes a conductive layer 225 in the same manner as the substrate 11. In the specification, a surface other than the first surface 215a and the second surface 215b among the surfaces that configures the substrate 215 is defined as a “side surface”.

[0062]

A penetration section 220 that is hollowed out from the first surface 215a to the second surface 215b of the substrate 215 is provided in the main board 205, and the main board 205 includes the interface section 221 that is electrically connected to the semiconductor device 1. A surface that configures the penetration section 220 in the substrate 215 is referred to as a “side surface” by the definition described above.

[0063]

The penetration section 220 has the same shape as, for example, the appearance of the semiconductor device 1, as illustrated in FIG. 10. That is, the main board 205 includes a plurality of first convex sections 221a that respectively meshes the plurality of first concave sections of the connector section 21, and a plurality of second convex sections 222 respectively mesh the plurality of second concave sections 22, in such a manner that the penetration section 220 has the same shape as the substrate 11.

[0064]

The interface section 221 includes the plurality of first convex sections 221a as described above. In addition, the interface section 221 has a structure in which a surface of the conductive layer 225 of the substrate 215 is partially exposed, and a plurality of second plating sections 221b is applied on the surface of the exposed conductive layers 225 in side surfaces of the first convex sections 221a, in the same manner as in a case of the substrate 11. The second plating sections 221b are also plated with, for example, gold in the same manner as in the first plating sections 21b, but are not limited to this. The first concave sections 21a on which plating is applied are meshed with and are in contact with the first convex sections 221a on which plating is applied in the same manner, and thereby the semiconductor device 1 is electrically connected to the host device 201. In addition, the gold plating is not necessarily required, and the conductive layer 225 may be in contact with the connector section 21 as it is in an exposed state.

[0065]

In addition, the interface section 221 may have a structure in which an elastic material 310, such as rubber or urethane is included between the second plating section (second metal section) 221b and the side surface of the substrate 215, in a state of being electrically connected to the conductive layer 225, in the same manner as in the connector section 21 described above.

[0066]

In this case, the connector section 21 is pressed by the interface section 221 according to the elastic force of the elastic material 310, and thereby stability of electric connection is increased.

[0067]

In addition, in the present embodiment, the first two plating sections 21b are provided in one of the first concave section 21a, but at this time, the first two plating sections 21b that face each other treats the same type of signals as each other, that is, it is preferable that signals which are treated in one concave section are one type. In this case, one of the first two plating sections 21b that face each other may be in contact with the second plating section 221b of the first convex section 221a that is provided on the substrate 215 of the main board 205, and stability of an electrical connection can be increased.

[0068]

In addition, the first plating section 21b need not be necessarily provided on the side surface of the first concave section 21a, and may be disposed in the first concave section 21a in a lateral direction of the substrate 11 as illustrated in FIG. 11, for example. In this case, a pressing section 301 is provided on a side opposite to the interface section 221, in the penetration section 220 of the substrate 215, and thereby, it is possible to increase stability of an electrical connection between the substrate 11 and the main board 205. In addition, the first plating section 21b may be provided so as to cover the whole of the first concave section. In this case, the first plating sections 21b are provided on three surfaces that form the first concave section 21a, any one surface of those may be in contact with the second plating section 221b of the first convex section 221a, and thereby stability of an electrical connection is further increased. In each case, the second plating section 221b is provided in the first convex section 221a, so as to be in contact with the first plating section 21b that is provided in the first concave section 21a.

[0069]

Here, an elastic material such as rubber is used for the pressing section 301. By providing the elastic material in a thickness direction of the substrate 215, the substrate 11 (semiconductor device 1) that is fitted into the main board 205 is always in a state of being pressed on the interface section 221 side, and a more stable electrical connection can be made. The pressing section 301 is not limited to an elastic material that uses rubber, and for example, may be a mechanism that uses a spring. In addition, the pressing section 301 need not be necessarily provided on the substrate 215, and may be provided on the second edge section 11d side of the substrate 11.

[0070]

In addition, as illustrated in FIG. 4, the substrate 11 includes a plurality of screw holes 11e. The substrate 11 is also screwed to the second fixing sections 231 of the housing 202 in the same manner as in the main board 205, and thereby, the semiconductor device 1 can be fixed in the thickness direction of the substrate 11. Furthermore, the plurality of the first convex sections 221a and the plurality of the second convex sections 221b of the main board 205 are respectively meshed with the plurality of the first concave sections 21a and the plurality of the second concave sections 22 of the substrate 11, and thereby, the semiconductor device 1 is also fixed in the surface direction of the substrate 11, and when the semiconductor device 1 is fixed to the second fixing sections 231, it is possible to perform more stable working.

[0071]

In the present embodiment, the semiconductor device 1 is fixed to the second fixing sections 231, in a state in which the main board 205 is fixed to the first fixing sections 230, and at the same time as that, the connector section 21 and the interface section 221 are electrically connected to each other.

[0072]

In addition, in the present embodiment, fixing of the semiconductor device 1 and the main board 205 need not be necessarily performed using screws, and for example, may be performed by pinning, and may be performed using a material such as an adhesive. The mechanisms or shapes of the first fixing sections 230 and the second fixing sections 231 are changed in accordance with a fixing method.

[0073]

In each case, height dimension of the protrusion sections of the first fixing sections 230 and the second fixing sections 231 is assorted, and thereby, the connector section 21 and the interface section 221 according to the fixing of the semiconductor device 1 are in contact with each other, and are electrically connected. In addition, in the present embodiment, the first concave section 21a and the first convex section 221a need not be necessarily provided, and the connector section 21 and the interface section 221 may have configurations in which the plurality of the first plating section 21b and the plurality of second plating section 221b are respectively provided on the side surfaces of the substrate 11 only, or the side surfaces of the substrate 215.

[0074]

In addition, in the present embodiment, the second concave section 22 and the second convex section 222 need not be necessarily provided, but if the second concave section 22 and the second convex section 222 exist, it is possible to perform more stable working when the above-described semiconductor device 1 is screwed.

[0075]

Furthermore, in the present embodiment, convex sections may be provided on the substrate 11, concave sections may be provided on the substrate 215, and concave sections and convex sections may be provided together on the substrate 11 and the substrate 215.

[0076]

Here, a case is considered in which a semiconductor device is not fitted into a main board, and the semiconductor device is inserted into a slot that is provided on a surface of the main board. In this case, by inserting the semiconductor device into the slot that is provided in the main board, the semiconductor device and a host device are electrically connected to each other. In this case, the semiconductor device and the main board that are inserted into the slot are disposed so as to be arranged substantially in parallel. When a semiconductor package is embedded in a host device, an embedding space in which an embedding height of the semiconductor package that is embedded in the semiconductor device is considered is required, as illustrated in, for example, FIG. 5.

[0077]

In addition, an embedded multi media card (eMMC) in which a NAND memory and a controller are incorporated into one package can be embedded in a main board and be used. In this case, the host device can be thinned, but in general, the operation speed of the eMMC is not as fast as that of an SSD, and in addition, exchange of components is extremely difficult.

[0078]

Thus, the present embodiment has a structure in which the semiconductor device 1 is fitted into the penetration section 220 of the main board 205. According to this configuration, the main board 205 and the substrate 11 exist on substantially the same plane. Thus, the semiconductor device 1 is contained in a space required for embedding the main board 205, in the thickness direction of the host device 201, and thereby the host device 201 can be thinned.

[0079]

Furthermore, in the present embodiment, the semiconductor device 1 and the main board 205 do not overlap each other. For this reason, it is possible to mitigate that heat which is generated from a component (for example, controller 13) embedded on the semiconductor device 1 affects the main board 205 through the air.

[0080]

In addition, the height of the semiconductor package, such as the NAND memory 12 or the controller 13 which is embedded on the substrate 11 is also substantially the same as that of a plurality of circuit components 216 that is embedded on the main board 205, and thus an embedding space need not be increased by taking into account an amount of protrusion of a component that is embedded on the substrate 11, saving of a space in which the main board 205 and the semiconductor device 1 are embedded can be made, and the host device 201 can be thinned.

[0081]

Furthermore, the semiconductor device 1 according to the present embodiment is a device of single-sided embedding. Thus, also in a point in which a protruded electronic component is not provided on a rear surface, an embedding space of the host device 201 in which the semiconductor device 1 is embedded is decreased, and accordingly the host device 201 can be thinned.

[0082]

In addition, as described above, even if an electronic component that is embedded in the semiconductor device 1 is embedded on the substrate 215 which directly configures the main board 205, the host device 201 can be thinned. However, in the present embodiment, the semiconductor device 1 is easily removed. Thus, also from a viewpoint of a performance test at the time of failure of components, or easiness of chip exchange, it can be said that the present embodiment is superior to a case in which the components, such as the NAND memory 12 or the controller 13 are directly embedded on the substrate 215.

[0083]

In addition, the present embodiment does not have a structure in which the semiconductor device 1 is inserted into a slot. Thus, a connection section that connectes the main board 205 to the semiconductor device 1 need not be configured along only the first edge section 11a of the substrate 11, and for example, may be provided in two edge sections adjacent to each other. In this case, it is possible to suppress concentration of wires in the periphery of the connector section 21, and degree of freedom of routing or the like of the wires in the semiconductor device 1 is increased. For this reason, electronic components, such as the NAND memory 12, the controller 13, and the DRAM 14 can also be more compactly disposed, and thus the semiconductor device 1 can also be miniaturized.

[0084]

Furthermore, in the same manner as also in the main board 205, wires through which the semiconductor device 1 and the host device 201 performs data communication need not be concentrated to one interface section 221, and degree of freedom of routing of wires or degree of freedom of component embedding is increased also in the main board 205.

[0085]

In addition, in the present embodiment, the connector section 21 and the interface section 221 do not embed components for connecting to each other and are provided on the side surfaces of the substrate 11 and the substrate 215. According to this configuration, not only the number of components that are used for realizing the host device 201 is reduced, but also a space for embedding components and wires according to the components need not be considered, the semiconductor device 1 and the main board 205 is miniaturized, and degree of design freedom is increased.

[0086]

Furthermore, in the present embodiment, the semiconductor device 1 is fixed to the housing 202 and at the same time as that, an electrical connection is made. Thus, it is not necessary to take a space into account, when designing, in order to perform an electrical connection, for example, to perform insertion and removal, and this also leads to a miniaturization of the host device 201.

[0087]

As described above, the first embodiment is described, but the embodiment of the semiconductor device 1 is not limited to this. Next, a semiconductor device according to a second embodiment will be described. The same symbols or reference numerals will be attached to the configuration having the same function as that of the first embodiment or having a similar function to the first embodiment, and description thereof will be omitted. In addition, configurations except for the configurations described below are the same as those of the first embodiment.

Second Embodiment

[0088]

The semiconductor device 1 according to the present embodiment is illustrated in FIG. 12. In FIG. 12, (a) is a plan view, (b) is a bottom surface view, and (c) is a side surface view. In addition, FIG. 13 is a sectional side view of the semiconductor device 1 and the main board 205 according to the present embodiment.

[0089]

The connector section 51 according to the present embodiment includes a stage 51a, as illustrated in FIG. 12 and FIG. 13. Since the substrate 11 is a multi-layer substrate, the number of layers of an area that configures the connector section 51 is smaller than that of other areas. That is, since the connector section 51 is processed in a thin manner, the stage 51a illustrated in FIG. 13 can be realized.

[0090]

In addition, in the stage 51a of the substrate 11, a first plating section (first metal section) 51b is provided on a surface that is substantially parallel with the first surface 11a of the substrate 11, and the first plating section 51b is electrically connected to the conductive layer 20 of the substrate 11 in the same manner as in the first embodiment.

[0091]

In addition, the main board 205 includes an interface section 251. The interface section 251 includes a stage 251a as illustrated in FIG. 13. In the same manner as in the substrate 11, the substrate 215 that configures the main board 205 is also a multi-layer substrate. Thus, by thinning a portion in the same manner as in the substrate 11 according to the present embodiment, the stage 251a can be provided.

[0092]

Furthermore, when the semiconductor device 1 is fitted into the penetration section 220, a second plating section (second metal section) 251b is provided on a surface that is in contact with the first plating section 51b, in the stage 251a. The plating sections are in contact with each other, and thereby the semiconductor device 1 and the host device 201 are electrically connected to each other.

[0093]

In the same manner as in the main board 205, the substrate 11 is also screwed to the housing 202, and thereby the semiconductor device 1 can be fixed in the thickness direction of the substrate 11. Furthermore, the stage 251a of the main board 205 and the plurality of the second convex sections 221b are respectively meshed with the stage 51a of the substrate 11 and the plurality of the second concave sections 22, and thereby the semiconductor device 1 is also fixed in a surface direction of the substrate 11.

[0094]

In addition, screw holes are provided in the stages 51b and 251b and the substrates 11 and 215 may be screwed to the housing 202. In this case, the first plating section 51b is pressed toward the second plating section 251b side by the screw, and thereby an electrical connection can be stable. It is preferable that screws which are used in this case is made of an insulating material such as plastic.

[0095]

In addition, the second concave section 22 and the second convex section 222 are provided in the substrate 11 and the main board 205 in the present embodiment, in the same manner as in the first embodiment. However, a method of fixing the semiconductor device 1 is not limited to this, and for example, the semiconductor device 1 may have the same structure as that of the stages that are provided in the connector section 51 and the interface section 251.

[0096]

In addition, also in the present embodiment, an elastic material may be interposed between the first metal section 51b and the substrate 11, in the same manner as in the first embodiment. In the present embodiment, a screw direction and a pressing direction of the elastic material substantially coincide each other, and thereby an electrical connection can be more stable.

[0097]

The present embodiment also has a configuration in which the semiconductor device 1 is positioned on substantially the same plane as the main board 205, a space in which the semiconductor device 1 and the main board 205 are embedded can be reduced, and the host device 201 can be thinned.

[0098]

In addition, the present embodiment also describes an example in which the semiconductor device 1 is fitted into the penetration section 220 of the substrate 215, but is not limited to this. In addition, the semiconductor device 1 is fixed to the second fixing sections 231 also in the present embodiment, and thereby the semiconductor device 1 and the main board 205 are electrically connected to each other.

Third Embodiment

[0099]

A sectional side view of the semiconductor device 1 and the main board 205 according to the present embodiment is illustrated in FIG. 14. A connector section need not be necessarily provided on the side surface of the substrate 11 as described in the first and second embodiments, and may be embedded on the first surface 11a of the substrate 11 as a connector component. In the same manner, an interface section that is provided in the main board 205 may also be embedded on the embedding surface 215a of the substrate 215.

[0100]

In the present embodiment, a connector section 61 and an interface section 261 are embedded together on the embedding surface 215a as a connector component. The connector section 61 and the interface section 261 respectively include a metal section 61a and a metal section 261a on an upper surface of a component (a surface on a side opposite to the embedding surface 215a). In addition, as illustrated in FIG. 14, the connector section 61 and the interface section 261 are covered by a cover 302.

[0101]

A sectional view of the connector section 61, the interface section 261, and the cover 302 is illustrated in FIG. 15. As illustrated in FIG. 15, a conductive section 302a is provided in an inner side of the cover 302, and the metal section 61a provided in the connector section 61 and the metal section 261a provided in the interface section 261 are electrically connected to each other via the conductive section 302a provided in the cover 302.

[0102]

In the present embodiment, the metal section 61a and the metal section 261a are provided with, for example, multiple pieces, may be configured to be respectively connected by a plurality of the conductive sections 302a that is provided so as to connect each other. As illustrated in FIG. 16, when the connector section 61 and the interface section 261 are covered by the cover 302, the metal sections 61a and 261a of a male terminal shape are inserted into the conductive sections 302a of a female terminal shape, and may be configured to be electrically and respectively connected by a conductive layer (not illustrated) that is provided in the inside of the cover 302.

[0103]

In addition, plating sections of the connector section 61 and the interface section 261 according to the present embodiment may be provided on side surfaces thereof in a state in which the plating sections are in contact with each other. In this case, the semiconductor device 1 is fixed to the second fixing sections 231, and thereby the connector section 61 and the interface section 261 are in contact with each other, and are electrically connected to each other. In addition, the connector section 61 and the interface section 261 are fixed to each other in a state of being pressed by the cover 302, and stability of an electrical connection is maintained.

[0104]

In addition, in the present embodiment, the connection section is configured to protrude on each of the embedding surface sides with respect to the substrate 11 and the substrate 215, differently from the connector section and the interface section according to the first and second embodiments. However, as illustrated in FIG. 14, since various electronic components including the NAND memory 12 are embedded on the substrate 11 and the substrate 215, if the connector section 61 and the interface section 261 are provided within a range of a height that is formed by protrusion of the various electronic components, the breadth of an embedding space need not be changed, and in the same manner as in the first and second embodiments, the host device 201 can be thinned.

Fourth Embodiment

[0105]

A connector section 71 of the semiconductor device 1 and an interface section 271 of the main board 205, according to the present embodiment are illustrated in FIG. 17.

[0106]

As illustrated in FIG. 17, a connector section 71 that is provided in the semiconductor device 1 includes a plurality of male terminals 71a. In addition, an interface section 271 that is provided on the embedding surface 215a of the substrate 215 includes a plurality of female terminals 271a that is the same pieces as the male terminals 71a described above, and an electrical connection is made by the male terminals 71a that are inserted into the female terminals 271a.

[0107]

Since an electrical connection according to the present embodiment is made by inserting terminals of a pin shape into each other, the present embodiment has a more electrically stable structure than a structure in which conductive materials (for example, plating materials) are merely in contact with each other.

[0108]

Furthermore, the connector section 71 and the interface section 271 in the present embodiment respectively have structures in which the embedding surface sides of the substrate 11 and the substrate 215 protrude, but as illustrated above, various electronic components including the NAND memory 12 are embedded on the substrate 11 and the substrate 215. Thus, if the connector section 71 and the interface section 271 are provided within a range of a height that is formed by protrusion of the various electronic components, the breadth of an embedding space need not be changed, and as a result, there is an effect that the host device 201 can be thinned.

Fifth Embodiment

[0109]

A view in which the semiconductor device 1 is embedded in a tablet type portable computer 201, according to the present embodiment, is illustrated in FIG. 18. In the present embodiment, the embedding surface 11a of the substrate 11 is positioned on a side opposite to the embedding surface 215a of the substrate 215 of the main board 205. Thus, in the semiconductor device 1 according to the present embodiment, a protruded component faces a side opposite to a display module.

[0110]

In the configuration described above, the semiconductor device 1 can avoid an affection of the heat that is generated in the display module, and the operation stability of the semiconductor device 1 can be increased. In addition, since the controller 13 and the housing 202 of the tablet type portable computer 201 are separated from each other, the heat emitted from the controller 13 is suppressed from being diffused to a surface of the tablet type portable computer 201, and it is possible to prevent surface temperature of the tablet type portable computer 201 from increasing. For this reason, stability of a user that uses the tablet type portable computer 201 is secured, and it is possible to increase convenience.

[0111]

In addition, the substrate 11 and the substrate 215 are positioned on substantially the same plane, also in the present embodiment. Thus, the semiconductor device 1 is contained in a space required for embedding the main board 205, in the thickness direction of the tablet type portable computer 201, and thereby the tablet type portable computer 201 can be thinned.

[0112]

In addition, a connection section that connects a connector section to an interface section in the present embodiment may have one of the configurations described in the first to fifth embodiments.

Sixth Embodiment

[0113]

The main board 205 according to the present embodiment is illustrated in FIG. 19. As illustrated in FIG. 19, a notch section 290 is provided in a substrate 216 of a substantially rectangular shape in the present embodiment. The semiconductor device 1 is embedded in a position of the notch section 290 as illustrated in FIG. 20.

[0114]

In addition, a connection section that connects a connector section to an interface section in the present embodiment may have one of the configurations described in the first to fifth embodiments. An example in which the connector section 21 and the interface section 221 that are described in the first embodiment are used is illustrated in FIG. 19 and FIG. 20.

[0115]

Since the configuration has a structure in which the substrate 11 and the substrate 215 are in parallel on substantially the same plane, the semiconductor device 1 is contained in a space required for embedding the main board 205, in the thickness direction of the host device 201, and thereby the hose device 201 can be thinned.

[0116]

In addition, the notch section 290 is provided in the present embodiment, but this configuration is also not necessarily required, the substrate 11 and the substrate 215 on which components are embedded may be respectively fixed in parallel only to the first fixing section 230 and the second fixing section 231. Also in this case, height dimension of the protrusion sections of the first fixing sections 230 and the second fixing sections 231 is assorted, and thereby, the host device 201 can be thinned. According to the fixing of the semiconductor device 1, the semiconductor device 1 and the main board 205 are electrically connected to each other.

[0117]

While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. An electronic apparatus comprising:

a housing in which a first fixing section and a second fixing section are provided;

a display device that is contained in the housing;

a memory device that is positioned in the housing;

a control device that controls the memory device;

a first substrate that is fixed to a first fixing section in a first position in the housing which overlaps the display device, includes a plurality of conductive layers which includes a first conductive layer, and includes a first exposition section which is electrically connected to the first conductive layer; and

a second substrate that overlaps the display device in parallel with the first substrate, is fixed to a second fixing section in a second position in the housing which is different from the first position, is in contact with the first exposition section according to fixing to the second fixing section, and includes a second exposition section which is electrically connected to the first exposition section.

2. The apparatus according to Claim 1,

wherein the second substrate includes a plurality of conductive layers including a second conductive layer,

wherein the second exposition section includes a metal section that covers at least a portion of the second conductive layer, and

wherein the metal section and the first exposition section are in contact with each other, according to fixing of the second substrate in the second position, and thereby the first substrate and the second substrate are electrically connected to each other.

3. The apparatus according to Claim 1 or 2, wherein a positioning section that positions the second substrate to the second position is provided in the housing.

4. The apparatus according to Claim 3,

wherein the positioning section is a first component that is provided on the second substrate and includes a first connection section which is electrically connected to the second exposition section, and

wherein at least a portion of the first connection section is in contact with at least a portion of the first exposition section and is electrically connected to at least a portion of the first exposition section, according to fixing of the second substrate.

5. The apparatus according to any one of Claims 1 to 4,

wherein the first exposition section is positioned on a first side surface of the first substrate, and

wherein the second exposition section is positioned on a second side surface of the second substrate.

6. The apparatus according to Claim 5,

wherein the positioning section is a first elastic section that is interposed between the metal section and the second substrate, and

wherein the first exposition section is pressed by the first elastic section, according to fixing of the second substrate in the second position, is in contact with the metal section, and is electrically connected to the metal section.

7. The apparatus according to Claim 5, wherein the positioning section is a first elastic section that is provided in at least a portion of the first substrate and presses the second exposition section toward the first exposition section, according to fixing of the second substrate in the second position.

8. The apparatus according to Claim 6 or 7,

wherein the second substrate includes at least one protrusion section on the second side surface, and

wherein at least a portion, that configures the protrusion section, of the second side surface is pressed toward at least a portion of the first side surface by the positioning section.

9. The apparatus according to any one of Claims 5 to 8, wherein at least a portion of the second side surface faces the first side surface.

10. An electronic apparatus comprising:

a housing in which a first fixing section and a second fixing section are provided;

a first substrate in which a first conductive section is provided and which is fixed to the first fixing section; and

a second substrate in which a second conductive section, that is electrically connected to the first conductive section, is provided, according to fixing of the second fixing section.

ABSTRACT

DRAWINGS

FIG. 1

201: HOST DEVICE

17: POWER SUPPLY CIRCUIT

13: CONTROLLER

12: NAND MEMORY

18: TEMPERATURE SENSOR

FIG. 6

12: NAND MEMORY

134: MEMORY INTERFACE SECTION

131: BUFFER

133: HOST INTERFACE SECTION